Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A data processing circuit for processing an input data pattern and for outputting an output data pattern ~~after a processing delay which depends on a processing activity of said data processing circuitry~~, said data processing circuitry comprising:

a) estimation means for estimating ~~said~~ a processing delay ~~based on~~ in response to said input data pattern, wherein the estimated processing delay corresponds to a delay that is caused as a function of a processing activity induced in said data processing circuit by said input data pattern; and

b) control means for controlling said processing of the input data pattern by said data processing circuit according to the processing activity of said data processing circuit in response to said estimated processing delay.

2. (original) A circuitry according to claim 1, wherein said estimation means comprises a look-up table for storing said estimated processing delay.

3. (original) A circuitry according to claim 2, wherein said look-up table is addressed by said input data pattern to output said estimated processing delay.

4. (previously presented) A circuitry according to claim 1, wherein said estimation means comprises a programmable delay line which is programmed by said input data pattern.

5. (original) A circuitry according to claim 4, wherein said programmable delay line is

adapted to generate an output signal after expiry of said estimated processing delay.

6. (previously presented) A circuitry according to claim 1, wherein said estimation means is adapted to estimate said processing delay based on a sequence of input data patterns.

7. (previously presented) A circuitry according to claim 1, wherein said control means is arranged to derive said processing activity from said estimated delay, and to control power supply of said data processing circuitry in response to said derived processing activity.

8. (previously presented) A circuitry according to claim 1, wherein said control means is adapted to control the clock supply to said data processing circuitry in response to said estimated processing delay.

9. (original) A circuitry according to claim 8, wherein said data processing circuitry has a pipeline structure and said control means is adapted to selectively gate said clock supply for each stage of said pipeline structure.

10. (original) A circuitry according to claim 9, wherein said control means is arranged to un-gate said clock supply if the previous stage has produced a valid output signal and the following stage has stored said output signal.

11. (previously presented) A circuitry according to claim 1, wherein said estimated processing delay is expressed as a number of cycles of said clock signal.

12. (currently amended) A method of controlling processing of an input data pattern and for outputting an output data pattern in a data processing circuit, ~~wherein a predetermined output data pattern is generated after a processing delay which depends on an activity of said processing,~~ said method comprising ~~the steps of~~:

a) estimating ~~said~~ a processing delay ~~based on~~ in response to said input data pattern, wherein the estimated processing delay corresponds to a delay that is caused as a function of a processing activity induced in the data processing circuit by said input data pattern; and

b) controlling a performing of said processing ~~control~~ of the input data pattern by the data processing circuit according to the processing activity of the data processing circuit in response to said estimated processing delay.

13. (currently amended) A method according to claim 12, wherein said ~~processing control is~~ controlling further includes a power control based on an activity monitoring of the processing activity of the data processing circuit.

14. (currently amended) A method according to claim 12, wherein said ~~processing control is~~ controlling further includes a control of a clock supply to a synchronous pipeline structure of the data processing circuit.